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ModelSim - Intel FPGA  
Edition Simulation  
Quick-Start: Intel  
Quartus Prime  
Standard Edition Send

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Feedback 10. Send  
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(Optional) Run  
Simulation at  
Command Line. Follow  
these steps to generate a  
.do. file that runs the  
ModelSim - Intel FPGA  
Edition simulator from  
the command line. 1.  
To open the example  
design project, click File  
Open ...

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ModelSim SE User ' s  
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and the reader should, in all cases, consult Mentor Graphics to determine whether any changes have been made.

ModelSim SE User ' s Manual	
ModelSim SE User ' s Manual Managing library contents . . . . .	
. . . . .	
UM-40 Assigning a	

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logical name to a design  
library . . . . .  
. . . . . UM-43

### ModelSim SE User ' s Manual

1. The VoptFlow  
modelsim.ini variable  
(below) sets the default  
design optimization on  
(1) or off (0). 2.

Optimized designs  
simulate faster, while  
non-optimized designs

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provide object visibility for debugging. 3. Use +acc with vopt or vsim -voptargs with +acc for selective design object visibility during debugging. 4.

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- UCSD

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University

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“ Recording Simulation  
Results With Datasets ”  
in the User ' s Manual  
for more information.

- datasetSeparator — is  
the character used to  
terminate the dataset

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name. The default is colon ( : ), though a different character (other than backslash ( \ )) may be specified as ...

## ModelSim Reference Manual - Computer Science

This manual uses the following conventions to define ModelSim command syntax.

## Documentation



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**Conventions** The following conventions are used to define ModelSim command syntax Table 1-1.

Conventions for Command Syntax	Syntax notation	Description
< >	angled brackets	surrounding a syntax item indicate a user-defined argument;
...	do not enter the ...	

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## Modelsim User

### ModelSim Command Reference Manual - Microsemi

You can edit, recompile, and re-simulate without leaving the ModelSim environment. All user interface operations can be scripted and simulations can run in batch or interactive modes. ModelSim simulates behavioral, RTL, and gate-level

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VITAL and Verilog  
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timing provided by the  
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menu, point to PDF  
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Manual. Modifying  
Stimulus Waveforms To  
modify stimulus  
waveforms, follow these  
steps: 1. Click in the

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waveform window to enable the Wave menu.  
2. On the Wave menu, point to Mouse Mode and then click Edit Mode. Make sure

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User Guide  
ModelSim / Questa  
Core: HDL Simulation  
teaches you to  
effectively use  
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Core to verify VHDL,  
Verilog, SystemVerilog,  
and mixed HDL  
designs. You. FPGA  
HDL & Other  
Languages Questa &  
ModelSim. View.  
2/3/21 — 2/4/21. 1  
other dates. Bangalore,  
India

Questa & ModelSim -  
Mentor Graphics

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Mentor Graphics  
ModelSim Simulator  
2019.4 Yes Cadence  
Incisive Enterprise  
Simulator (IES)  
15.20.079 Yes Synopsys  
Verilog Compiler



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### Simulator (VCS)

P-2019.06-SP1-1 Yes ...

- Vivado Design Suite

User Guide: Design

Flows Overview

(UG892) Simulation

Flow.

Guide: Logic Simulation  
- Xilinx

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programmable gate  
array is a semiconductor  
integrated circuit where  
electrical functionality is  
customized to accelerate  
key workloads.

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